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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/489,652	01/24/2000	William G. Burroughs	KUC-718US	6089

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EXAMINER	
TANG, KENNETH	
ART UNIT	**PAPER NUMBER**
2127	2

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

RR4

Office Action Summary	Application No.	Applicant(s)	
	09/489,652	BURROUGHS ET AL.	
	Examiner	Art Unit	
	Kenneth Tang	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 1/24/00

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-6, 8-9, 11, 13-14, 16-20, and 22-26 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Anderson (US 5,581,748).

3. As to claim 1, Anderson teaches a system having first and second processors, a method 2 of synchronizing the first processor with the second processor (see Abstract), comprising the steps of:

- (a) storing in a register parallel bits of data from the first processor, wherein at least one bit of data is a logic ONE *(col. 8, lines 33-34)*,
- (b) forming an output signal from the at least one bit of data in the register *(col. 11, lines 22-27)*, and

- (c) sending the output signal to an interrupt terminal of the second processor for synchronizing the first processor with the second processor *(col. 10, lines 36-38 and col. 11, lines 22-27)*.

4. As to claim 2, Anderson teaches wherein the register is a memory mapped register *(col. 6, lines 37-49)*.

5. As to claim 4, Anderson teaches wherein at least one of the first and second processors is a digital signal processor (DSP) *(see Abstract)*.

6. As to claim 5, Anderson teaches the wherein step (b) includes detecting a leading edge of the at least one bit of data to form the output signal *(col. 11, lines 22-27)*.

7. As to claim 6, Anderson teaches wherein step (c) includes sending the output signal on a dedicated line between the register and the interrupt terminal *(Fig. 4 and col. 15, lines 40-47)*.

8. As to claim 8, Anderson teaches the method including the steps of enabling the register during a write cycle, and storing the parallel bits of data when an address of the register matches a predetermined address *(col. 6, lines 37-49)*.

9. As to claim 9, Anderson teaches a system for providing an interrupt signal from a first processor to a second processor comprising a data bus coupled to the first processor for routing

parallel bits of data *(col. 5, lines 9-12)*, a register coupled to the data bus for storing the parallel bits of data *(col. 6, lines 37-39)*, at least one of the parallel bits of data having an active logic level *(col. 8, lines 33-34)*, an edge detector coupled to the register for detecting active logic levels stored in the register and converting each active logic level into an interrupt signal *(col. 11, lines 22-27)*, and at least one line coupled between the edge detector and an interrupt terminal of the second processor for routing one of the interrupt signals to the interrupt terminal *(col. 5, lines 9-12, and col. 6, lines 41-43)*.

10. As to claim 11, Anderson teaches further including an address bus coupled between the first processor and the register *(see rejection of claim 9)*, and a predetermined address for the register, wherein the first processor routes the parallel bits of data to the register by setting the predetermined address on the address bus *(col. 6, lines 37-49)*.

11. As to claim 13, it is rejected for the same reasons as stated in the rejection of claim 4.

12. As to claim 14, Anderson teaches having data lines between each processor and at least one interrupt terminal in each processor *(col. 10, lines 36-38 and col. 11, lines 22-27)*, a system for synchronizing a first processor with a second processor comprising a register coupled to the data lines for storing data bits from the first processor *(col. 11, lines 22-27)*, each data bit representing an interrupt signal *(col. 11, lines 22-27)*, a detector for detecting each of the data bits in the register *(see Abstract)*, and a signal router for routing each of the detected data bits to a respective interrupt terminal in the second processor *(col. 8, lines 3-4)*, wherein when the first

processor stores a data bit in the register, the router provides an interrupt signal to the second processor *(col. 11, lines 22-27)*.

13. As to claim 16, Anderson teaches wherein the signal router includes a set of lines, each line connected to the respective interrupt terminal *(Fig. 4 and col. 15, lines 40-47)*.

14. As to claim 17, it is rejected for the same reasons as stated in the rejection of claim 4.

15. As to claim 18, Anderson teaches further including an address bus coupled to the register, wherein the data bits are stored in the register when the first processor addresses the register *(col. 6, lines 37-49)*.

16. As to claim 19, Anderson teaches wherein the data bits are stored in the register during a first clock cycle and the data bits are detected by the detector during a second clock cycle, and the interrupt signal is enabled for a duration of a clock cycle *(col. 15, lines 12-14)*.

17. As to claim 20, it is rejected for the same reasons as stated in the rejection of claim 14. In addition, Anderson teaches teaches an integrated circuit including at least two processors *(see Abstract)*, data lines between each processor *(col. 4, lines 54-55)*, and at least one interrupt terminal in each processor *(It is inherent that processors have interrupts)*.

18. As to claim 22, it is rejected for the same reasons as stated in the rejection of claim 16.

19. As to claim 23, it is rejected for the same reasons as stated in the rejection of claim 4.

20. As to claim 24, Anderson teaches wherein at least one processor is a microprocessor *(see Abstract)*.

21. As to claim 25, it is rejected for the same reasons as stated in the rejection of claim 18.

22. As to claim 26, it is rejected for the same reasons as stated in the rejection of claim 19.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 7, 10, 15, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US 5,581,748).

24. As to claim 7, it is well known in the art that output signals can be active for a duration of a clock period because it aids in scheduling and synchronization.

25. As to claim 10, Anderson teaches the use of registers and an edge detector but fails to explicitly teach using flip flops for them. However, it is well known in the art that using flip flops because flip flops are standard to alter the state when a current is applied to a circuit (for example, 1 to 0, or 0 to 1).

26. As to claim 15, it is rejected for the same reasons as stated in the rejection of claim 10.

27. As to claim 21, it is rejected for the same reasons as stated in the rejection of claim 10.

28. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US 5,581,748) in view of Burroughs et al. (hereinafter Burroughs) (US 6,691,190 B1).

29. As to claim 3, Anderson fails to explicitly teach wherein the register is an off-core register. However, Burroughs teaches data exchanges between multiple DSPs using an off-core and memory-mapped registers *(see Claim 6 and col. 5, lines 1-18)*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of off-core registers to the existing DSP synchronization system because it allows for direct access to the registers.

30. As to claim 12, it is rejected for the same reasons as stated in the rejection of claims 3 and 8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (703) 305-5334. The examiner can normally be reached on 8:30AM - 7:00PM, Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kt
3/8/04

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